REMARKS

The present filing is responsive to the Office Action.

Summary of the Response

Claims 1 and 20 have been amended. Claims 3-8 have been previously canceled. Claims 1, 2 and 9-20 remain pending in this application. Reexamination and reconsideration of the present application as amended are respectfully requested.

Allowable Subject Matter

Applicant appreciates the Examiner's allowance of claims 2 and 9-19, and the indication of allowable subject matter in claims 20-24. Claim 20 has been rewritten into independent form, incorporating all the limitations of claim 1.

Claim Rejections Under 35 USC 102

Claims 1 is rejected under 35 U.S.C. 102(b) as being anticipated by the Aoki et al. (US Patent No. 5,192,879). This rejection is respectfully traversed.

Claim 1 as amended requires a voltage dropping circuit dropping voltages on a first node located between said first input portion and said first output portion to ground voltage and on a second node located between said second input portion and said second output portion to ground voltage, before changing from a state in which said first input portion is disconnected from said first node to a state in which said first input portion is connected to said first node, wherein in the state in which said input portion is connected to the first node, the first node and the second node have complementary high and low voltages. Aoki does not disclose the recited voltage dropping

circuit dropping voltages on the recited first and second nodes, and such complementary high and low voltages at the recited first and second nodes in the recited state. In the embodiment of the present invention illustrated in Fig. 3, the first and second nodes N1 and N2 are connected to the input terminal and output terminals of the inverter, respectively. As shown in Fig. 4, in the state in which said said input portion is connected to the first node, i.e., after the TFTs 5 and 6 are turned off and the TFTs 2 and 3 are turned on, the input signals Si1 and Si2 are output to the input terminals of the inverters 11 and 12, respectively. As a result, the first node and the second node have complementary high and low voltages, according to the first input signal Si1 because of the inverter 11.

In contradistinction, in Aoki, Fig. 4, the source terminals of the MOS transistors 2N and 2P and the drain terminals of the MOS transistors 1N and 1P are connected to the output terminal 12. When the input terminal 11 is at L level, the MOS transistors 2N and 1P are both turned on to pull the output terminal 12 to the power voltage Vdd. However, that being the case, in the state in which the input portion is connected to the first node, the voltage on the source terminals of the MOS transistor 2N and 2P (i.e., alleged first node) is identical to that on the drain terminals of the MOS transistors 1N and 1P (i.e., alleged second node), rather than complementary high and low voltages. Further, even if the voltage on the source terminals of the MOS transistors 2N and 2P and the voltage on the source terminals of the MOS transistors 1N and 1P, are somehow deemed to be at complementary high and low voltages, there would be a leakage current flowing through the power voltage Vdd to the ground voltage, which could render the structure of Aoki inoperable in the voltage converting device of the present invention. Accordingly, Aoki does not teach the voltage converting device recited in claim 1 as amended.

CONCLUSION

In view of all the foregoing, Applicant submits that the claims pending in this application are patentable over the references of record and are in condition for allowance. Such action at an early date is earnestly solicited. **The Examiner is invited to call the undersigned representative to discuss any outstanding issues that may not have been adequately addressed in this response.**

The Assistant Commissioner is hereby authorized to charge any additional fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this transmittal and associated documents, or to credit any overpayment to **Deposit Account No. 501288** referencing the attorney docket number of this application.

Respectfully submitted,

/Wen Liu; 32,822/

Dated: June 23, 2008

Wen Liu
Registration No. 32,822

LIU & LIU
444 S. Flower Street; Suite 1750
Los Angeles, California 90071
Telephone: (213) 830-5743
Facsimile: (213) 830-5741
Email: wliu@liulaw.com